| I.C. TYPE | +5V (PIN) | GND | -5V (PIN) | DESIGNATIONS | SPARE GATES |
|---|---|---|---|---|---|
| 74S00 | 14 | 7 | | U6,9,17 | U9 - A,D , U6 - B,D |
| 74S02 | 14 | 7 | | U15 | U15 - A |
| 74LS02 | 14 | 7 | | U18 | U18 - B |
| 74S04 | 14 | 7 | | U1,29,95 | U1-A-C,E,F , U29-A |
| 74LS04 | 14 | 7 | | U32,101,104,122, 127 | |
| 7407 | 14 | 7 | | U35 | U35 - E |
| 74S08 | 14 | 7 | | U3,96 | |
| 74LS08 | 14 | 7 | | U38,42 | |
| 74S10 | 14 | 7 | | U2,23,30 | U2 - B |
| 74S11 | 14 | 7 | | U78 | |
| 74LS11 | 14 | 7 | | U33 | U33 - C |
| 74LS14 | 14 | 7 | | U81 | |
| 74S20 | 14 | 7 | | U7,31 | U7 - B |
| 74LS21 | 14 | 7 | | U4,37 | |
| 74LS27 | 14 | 7 | | U54 | |
| 74S32 | 14 | 7 | | U21 | |
| 74LS32 | 14 | 7 | | U8,22,27,41 | U8 - C,D , U27 - C,D |
| 74S51 | 14 | 7 | | U16 | |
| 74S74 | 14 | 7 | | U5,13,97 | |
| 74LS74 | 14 | 7 | | U28,40 | |
| 74S85 | 14 | 7 | | U52,53 | |
| 74S113 1) | 14 | 7 | | U14,20,83 | |
| 74LS133 | 16 | 8 | | U45 | |
| 74LS138 2) | 16 | 8 | | U24-26,39,55 | |
| 74LS175 | 16 | 8 | | U36 | |

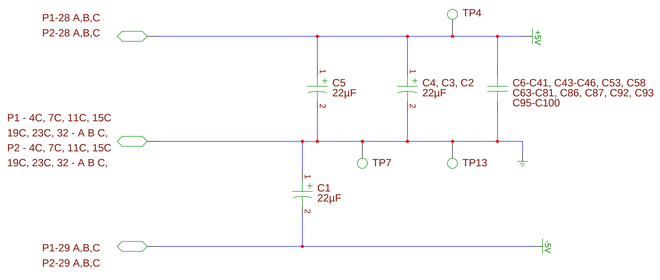
1) U83 is a LS on my board
2) U25 and U26 are both S on my board

3

| I.C. TYPE | +5V (PIN) | GND | -5V (PIN) | DESIGNATIONS | SPARE GATES |
|---|---|---|---|---|---|
| 74S240 | 20 | 10 | | U11,68,109 | |
| 74S241 | 20 | 10 | | U99 | |
| 74LS244 | 20 | 10 | | U12,51,67,73,103, 108,110,112,114-118 | |
| 74LS245 | 20 | 10 | | U46,63.111,113 | |
| 74S260 | 14 | 7 | | U34 | U34 - A |
| 74LS260 | 14 | 7 | | U61 | U61 - B |
| 74S373 | 20 | 10 | | U47,62,71,72 | |
| 74LS374 | 20 | 10 | | U48,49,50,65,66 | |
| 26LS30 | 1 | 5 | 8 | U100,102,105,124, 126,128 | |
| 26LS32 | 16 | 8 | | U106,107,120, 121,123,125 | |
| 93S16 | 16 | 8 | | U98 | |
| Z80B-CTC | 25 | 5 | | U43,44,89 | |
| 2114(p)-3 | 18 | 9 | | U57-60 | |
| Z8001A-CPU | 11 | 36 | | U64 | |
| 2732 | 24 | 12 | | U74-77 | |
| Z80CLK DRV | 1 | 5 | | U79,80 | |
| 2.4576 MHz | 14 | 7 | | U84 | |
| 44.440 MHz | 14 | 7 | | U85 | |
| Z8010A MMU | 11 | 35 | | U86,87,88 | |
| Z80B-SIO/2 | 9 | 31 | | U90-93 | |
| Z80B-PIO | 26 | 11 | | U94 | |
| | | | | | |

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IKa, 1/4W, 5%
2. CAPACITOR VALUES ARE IN MICROFARADS.
3. ALPHANUMERIC DENOTES GATES.



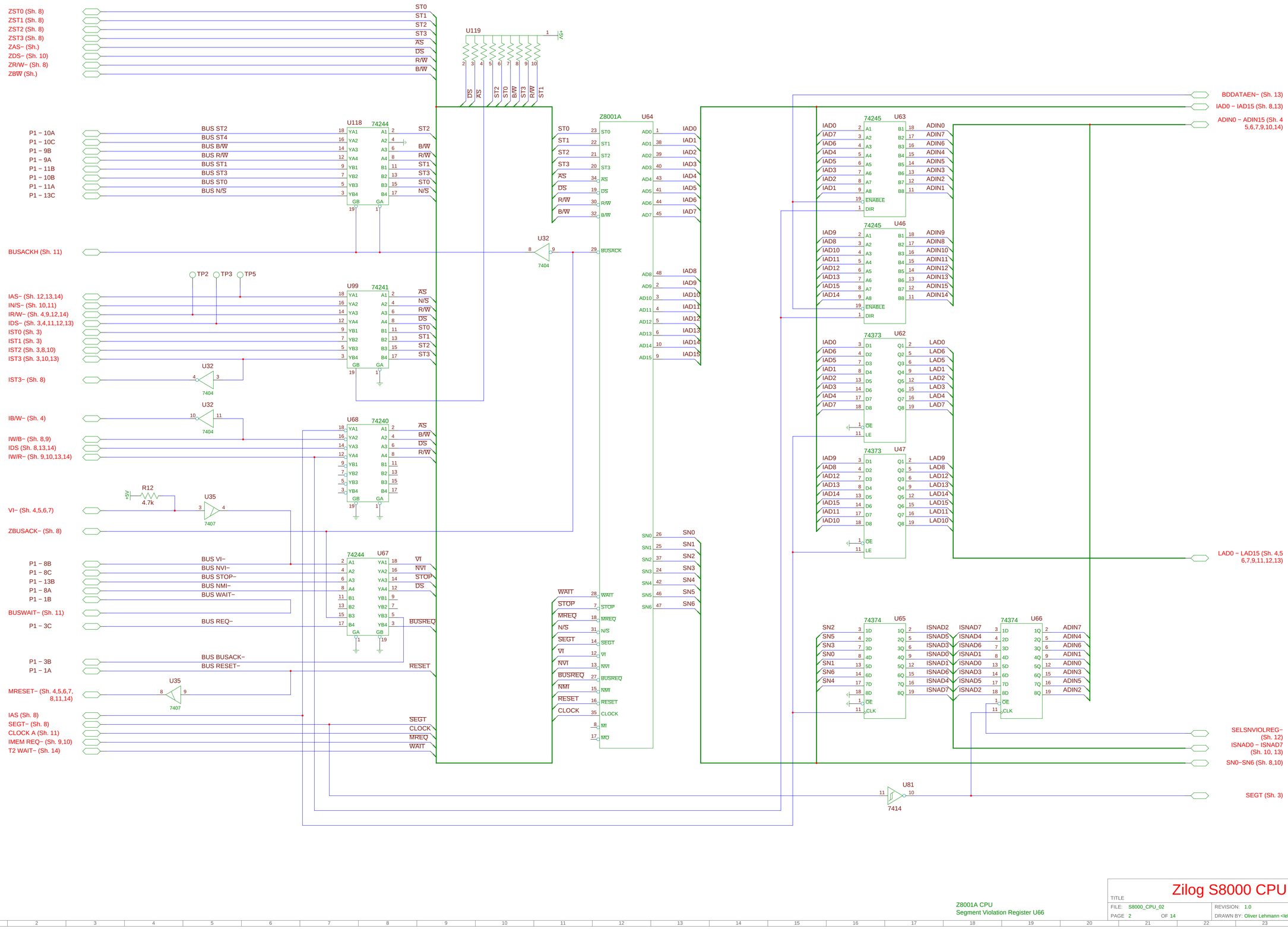

| REF DESIGNATION | |
|---|---|
| LAST USED | NOT USED |
| C100 | ——— |
| CR1 | ——— |
| DS4 | ——— |
| R20 | ——— |
| U128 | ——— |

# Zilog S8000 CPU

TITLE

FILE: S8000_CPU_01 REVISION: 1.0

PAGE 1 OF 14 DRAWN BY: Oliver Lehmann <lehmann@ans-netz.de>




Z8001A CPU
Segment Violation Register U66

# Zilog S8000 CPU

TITLE

FILE: S8000_CPU_02 REVISION: 1.0

PAGE 2 OF 14 DRAWN BY: Oliver Lehmann <lehmann@ans-netz.de>

IAD0 – IAD15 (Sh. 2)

IF1LOBYTE– (Sh. 12)

TRPLOBYTE– (Sh. 12)

SEGT (Sh. 2)

IST0 (Sh. 2)

IST1 (Sh. 2)

IST2 (Sh. 2)

IST3 (Sh. 2)

NMI SWITCH (N.O.) P2 – 26C

NMI SWITCH (N.C.) P2 – 25C

MANUAL NMI (Sh. 10)

LATCHECCERROR (Sh. 4)

POWERFAIL (Sh. 10,11)

IDS– (Sh. 2)

74374 U48

74374 U50

74374 U49

IAD7 IAD6 IAD5 IAD4 IAD1 IAD2 IAD3 IAD0

ADIN7 ADIN6 ADIN5 ADIN4 ADIN3 ADIN2 ADIN1 ADIN0

ADIN0 – IADIN7 (Sh. 2)

U27 7432

74138 U25

74138 U26

R4 1k +5V

R2 1k +5V

R3 1k +5V

U9 7400

U9 7400

U4 7421

U54 7427

U35 7407

TP6

U8 7432

U8 7432

I/O REF– (Sh. 11,12)

SEGTACK (Sh. 8)

VIACK– (Sh. 12)

MMU/EPUREF– (Sh. 13)

STACKMEMREQ– (Sh. 4)

INSTFETCH1STWD– (Sh.8)

EPUXFER– (Sh. 11)

BUS NMI–

P1 – 8A

ONBDNMI– (Sh. 12)

ENAONBDNMI– (Sh. 10)

External Violation Registers (U48,49,50)
VIACK– generation

# Zilog S8000 CPU

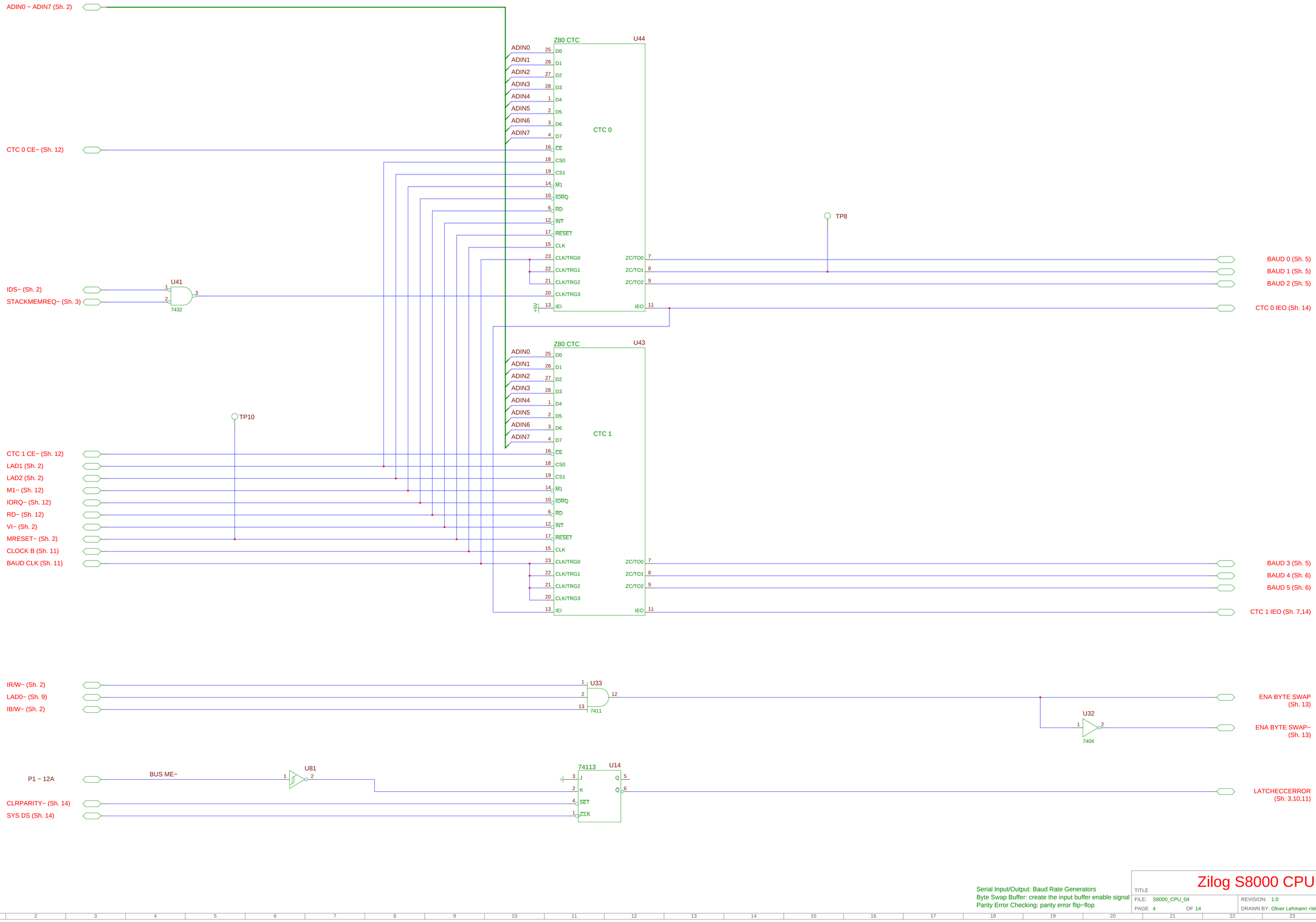
TITLE

FILE: S8000_CPU_03

REVISION: 1.0

PAGE 3 OF 14

DRAWN BY: Oliver Lehmann <lehmann@ans-netz.de>




Serial Input/Output: Baud Rate Generators
Byte Swap Buffer: create the input buffer enable signal
Parity Error Checking: parity error flip–flop

# Zilog S8000 CPU

TITLE

FILE: S8000_CPU_04

REVISION: 1.0

PAGE 4 OF 14

DRAWN BY: Oliver Lehmann <lehmann@ans-netz.de>

ADIN0 ~ ADIN7 (Sh. 2)

SIO 0 CE~ (Sh. 12)

CTC 2 IEO (Sh. 7,14)

BAUD 0 (Sh. 4)

BAUD 1 (Sh. 4)

LAD1 (Sh. 2)

LAD2 (Sh. 2)

SIO 1 CE~ (Sh. 12)

MRESET~ (Sh. 2)

M1~ (Sh. 12)

IORQ~ (Sh. 12)

RD~ (Sh. 12)

CLOCK B (Sh. 11)

VI~ (Sh. 2)

BAUD 2 (Sh. 4)

BAUD 3 (Sh. 4)

U119 Pin 4 (Sh. 2)

Z80 SIO/2 U92

SIO 0

ADIN0 40 D0 — W/RDYA 10
ADIN1 1 D1 — DTRA 16
ADIN2 39 D2 — RTSA 17
ADIN3 2 D3 — TxDA 15
ADIN4 38 D4 — DCDA 19
ADIN5 3 D5 — CTSA 18
ADIN6 37 D6 — RxDA 12
ADIN7 4 D7 — SYNCA 11
B/A 34 — W/RDYB 30
C/D 33 — DTRB 25
CE 35 — RTSB 24
RESET 21 — TxDB 26
M1 8 — DCDB 22
IORQ 36 — CTSB 23
RD 32 — RxDB 29
CLK 20
INT 5
IEI 6
IEO 7
RXCA 13
TXCA 14
RXCB 28
TXCB 27

U127 7404 (1,2) — U128 26ls30 (1,15) C94 (16) — DSR0 — P2 ~ 4A
U127 7404 (11,10) — U128 26ls30 (6,11) C96 (12) — CTS0 — P2 ~ 2B
U127 7404 (9,8) — U128 26ls30 (7,10) C97 (9) — RXD0 — P2 ~ 1B
U107 26ls32 (13,15) C98 (14) — DTR0 — P2 ~ 3B
U107 26ls32 (3,1) C99 (2) — RTS0 — P2 ~ 3A
U107 26ls32 (11,9) C100 (10) — TXD0 — P2 ~ 2A
TXRTN0 — P2 ~ 1A

U127 7404 (5,6) — U126 26ls30 (7,10) C91 (9) — DSR1 — P2 ~ 7A
U127 7404 (3,4) — U126 26ls30 (2,15) C88 (16) — CTS1 — P2 ~ 5B
U127 7404 (13,12) — U128 26ls30 (3,14) C95 (13) — RXD1 — P2 ~ 4B
U106 26ls32 (13,15) C101 (14) — DTR1 — P2 ~ 6B
U106 26ls32 (11,9) C102 (10) — RTS1 — P2 ~ 6A
U107 26ls32 (5,7) C103 (6) — TXD1 — P2 ~ 5A
TXRTN1 — P2 ~ 14C

SIO 0 IEO (Sh. 14)

Z80 SIO/2 U92

SIO 1

ADIN0 40 D0 — W/RDYA 10
ADIN1 1 D1 — DTRA 16
ADIN2 39 D2 — RTSA 17
ADIN3 2 D3 — TxDA 15
ADIN4 38 D4 — DCDA 19
ADIN5 3 D5 — CTSA 18
ADIN6 37 D6 — RxDA 12
ADIN7 4 D7 — SYNCA 11
B/A 34 — W/RDYB 30
C/D 33 — DTRB 25
CE 35 — RTSB 24
RESET 21 — TxDB 26
M1 8 — DCDB 22
IORQ 36 — CTSB 23
RD 32 — RxDB 29
CLK 20
INT 5
IEI 6
IEO 7
RXCA 13
TXCA 14
RXCB 28
TXCB 27

U104 7404 (3,4) — U126 26ls30 (3,14) C89 (13) — DSR2 — P2 ~ 10A
U104 7404 (1,2) — U105 26ls30 (2,15) C59 (16) — CTS2 — P2 ~ 8B
U104 7404 (11,10) — U126 26ls30 (6,11) C90 (12) — RXD2 — P2 ~ 7B
U125 26ls32 (13,15) C104 (14) — DTR2 — P2 ~ 9B
U106 26ls32 (5,7) C105 (6) — RTS2 — P2 ~ 9A
U106 26ls32 (3,1) C106 (2) — TXD2 — P2 ~ 8A
TXRTN2 — P2 ~ 18C

U104 7404 (9,8) — U105 26ls30 (7,10) C62 (9) — DSR3 — P2 ~ 13A
U104 7404 (13,12) — U105 26ls30 (3,14) C60 (13) — CTS3 — P2 ~ 11B
U104 7404 (5,6) — U105 26ls30 (6,11) C61 (12) — RXD3 — P2 ~ 10B
U125 26ls32 (3,1) C107 (2) — DTR3 — P2 ~ 12B
U125 26ls32 (5,7) C108 (6) — RTS3 — P2 ~ 12A
U125 26ls32 (11,9) C109 (10) — TXD3 — P2 ~ 11A
TXRTN3 — P2 ~ 26A

SIO 1 IEO (Sh. 14)

U105 26ls30 (16 VCC, 5 GND, 4 MODE, 8 Vee; +5V, -5V)
U126 26ls30 (16 VCC, 5 GND, 4 MODE, 8 Vee; +5V, -5V)
U128 26ls30 (16 VCC, 5 GND, 4 MODE, 8 Vee; +5V, -5V)
U106 26ls32 (4 Ctrl, 12 Ctrl, 16 VCC, GND 8; +5V)
U107 26ls32 (4 Ctrl, 12 Ctrl, 16 VCC, GND 8; +5V)
U125 26ls32 (4 Ctrl, 12 Ctrl, 16 VCC, GND 8; +5V)

Serial Input/Output: SIO channels 0 through 3

# Zilog S8000 CPU

TITLE

FILE: S8000_CPU_05 — REVISION: 1.0

PAGE 5 OF 14 — DRAWN BY: Oliver Lehmann <lehmann@ans-netz.de>

ADIN0 – ADIN7 (Sh. 2)

SIO 2 CE– (Sh. 12)

SIO 2 IEI (Sh. 14)

BAUD 4 (Sh. 4)

BAUD 5 (Sh. 4)

Z80 SIO/2 U91

SIO 2

ADIN0 40 D0 | 1 D1 | 39 D2 | 2 D3 | 38 D4 | 3 D5 | 37 D6 | 4 D7

34 B/A | 33 C/D | 35 CE | 21 RESET | 8 M1 | 36 IORQ | 32 RD | 20 CLK | 5 INT | 6 IEI | 7 IEO | 13 RxCA | 14 TxCA | 28 RxCB | 27 TxCB

W/RDYA 10 | DTRA 16 | RTSA 17 | TxDA 15 | DCDA 19 | CTSA 18 | RxDA 12 | SYNCA 11 | W/RDYB 30 | DTRB 25 | RTSB 24 | TxDB 26 | DCDB 22 | CTSB 23 | RxDB 29

U122 7404 (DTRA) | U122 7404 (RTSA) | U122 7404 (TxDA)

U124 26ls30 C82 | U124 26ls30 C84 | U124 26ls30 C85

U123 26ls32 | U123 26ls32 | U123 26ls32

DSR4 P2 – 16A

CTS4 P2 – 14B

RXD4 P2 – 13B

DTR4 P2 – 15B

RTS4 P2 – 15A

TXD4 P2 – 14A

TXRTN4 P2 – 27A

U122 7404 (DTRB) | U122 7404 (RTSB) | U122 7404 (TxDB)

U102 26ls30 C55 | U102 26ls30 C57 | U124 26ls30 C83

U121 26ls32 | U121 26ls32 | U123 26ls32

DSR5 P2 –19A

CTS5 P2 – 17B

RXD5 P2 – 16B

DTR5 P2 – 18B

RTS5 P2 – 18A

TXD5 P2 – 17A

TXRTN5 P2 – 25B

SIO 2 IEO (Sh. 14)

Z80 SIO/2 U90

SIO 3

LAD1 (Sh. 2)

LAD2 (Sh. 2)

SIO 3 CE– (Sh. 12)

MRESET– (Sh. 2)

M1– (Sh. 12)

IORQ– (Sh. 12)

RD– (Sh. 12)

CLOCK B (Sh. 11)

VI– (Sh. 2)

SIO 3 IEI (Sh. 14)

BAUD 6 (Sh. 7)

BAUD 7 (Sh. 7)

ADIN0 40 D0 | 1 D1 | 39 D2 | 2 D3 | 38 D4 | 3 D5 | 37 D6 | 4 D7

34 B/A | 33 C/D | 35 CE | 21 RESET | 8 M1 | 36 IORQ | 32 RD | 20 CLK | 5 INT | 6 IEI | 7 IEO | 13 RxCA | 14 TxCA | 28 RxCB | 27 TxCB

W/RDYA 10 | DTRA 16 | RTSA 17 | TxDA 15 | DCDA 19 | CTSA 18 | RxDA 12 | SYNCA 11 | W/RDYB 30 | DTRB 25 | RTSB 24 | TxDB 26 | DCDB 22 | CTSB 23 | RxDB 29

U101 7404 (DTRA) | U101 7404 (RTSA) | U101 7404 (TxDA)

U100 26ls30 C51 | U102 26ls30 C54 | U102 26ls30 C56

U120 26ls32 | U121 26ls32 | U121 26ls32

DSR6 P2 – 22A

CTS6 P2 – 20B

RXD6 P2 – 19B

DTR6 P2 – 21B

RTS6 P2 – 21A

TXD6 P2 – 20A

TXRTN6 P2 – 26B

U101 7404 (DTRB) | U101 7404 (RTSB) | U101 7404 (TxDB)

U100 26ls30 C49 | U100 26ls30 C50 | U100 26ls30 C52

U120 26ls32 | U120 26ls32 | U120 26ls32

DSR7 P2 – 25A

CTS7 P2 – 23B

RXD7 P2 – 22B

DTR7 P2 – 24B

RTS7 P2 – 24A

TXD7 P2 – 23A

TXRTN7 P2 – 27B

SIO 3 IEO (Sh. 14)

26ls30 U100 | 26ls30 U102 | 26ls30 U124 | 26ls32 U120 | 26ls32 U121 | 26ls32 U123

VCC 16 (+5V) | GND 5 | MODE 4 | Vee 8 (-5V) | Ctrl | Ctrl 12

U119 Pin 4 (Sh. 2)

Serial Input/Output: SIO channels 4 through 7

# Zilog S8000 CPU

TITLE

FILE: S8000_CPU_06

REVISION: 1.0

PAGE 6 OF 14

DRAWN BY: Oliver Lehmann <lehmann@ans-netz.de>

ADIN0 – ADIN7 (Sh. 2)

CTC 2 CE– (Sh. 12)

MRESET– (Sh. 2)

BAUD CLK (Sh. 11)

CTC 1 IEO (Sh. 4)

LAD1 (Sh. 2)

LAD2 (Sh. 2)

PIO CE– (Sh. 12)

M1– (Sh. 12)

IORQ– (Sh. 12)

RD– (Sh. 12)

CLOCK B (Sh. 11)

VI– (Sh. 2)

PIO 0 IEI (Sh. 14)

Z80 CTC U89

ADIN0 25 D0
ADIN1 26 D1
ADIN2 27 D2
ADIN3 28 D3
ADIN4 1 D4
ADIN5 2 D5
ADIN6 3 D6
ADIN7 4 D7

18 CS0
19 CS1
16 CE
17 RESET
14 M1
10 IORQ
6 RD
15 CLK
23 CLK/TRG0
22 CLK/TRG1 ZC/TO0 7
21 CLK/TRG2 ZC/TO1 8
20 CLK/TRG3 ZC/TO2 9
12 INT
13 IEI
11 IEO

BAUD 6 (Sh. 6)

BAUD 7 (Sh. 6)

CTC 2 IEO (Sh. 5)

U42 7408

Z80 PIO U94

ADIN0 19 D0
ADIN1 20 D1
ADIN2 1 D2
ADIN3 40 D3
ADIN4 39 D4
ADIN5 38 D5
ADIN6 3 D3
ADIN7 2 D7

6 B/A SEL
5 C/D SEL
4 CE
37 M1
36 IORQ
35 RD
25 CLK
23 INT
24 IEI
22 IEO

ARDY 18
ASTB 16
BRDY 21
BSTB 17

A0 15 A1
A1 14 A2
A2 13 A3
A3 12 A4
A4 10 A5
A5 9 A6
A6 8 A7
A7 7

B0 27 B0
B1 28 B1
B2 29 B2
B3 30 B3
B4 31 B4
B5 32 B5
B6 33 B6
B7 34 B7

E16 E18 E17 E14 E15 E13

U103 74244

A3 A1 A2 → 2 4 6 8 A1 A2 A3 A4 → Y1 Y2 Y3 Y4 18 16 14 12 → DA STROBE/DA STROBE–, M.U./INPUT PRIME
G 1

U103 74244

A6 A5 A7 → 9 7 5 3 Y1 Y2 Y3 Y4 → A1 A2 A3 A4 11 13 15 17 → IFVALID/FAULT–, ON–LINE/SELECT
G 19

R20 1k +5V
R19 1k +5V

U11 74240

9 → 11
19

R5 1k +5V → BUSY–

U108 74244

B0 B1 B2 B3 B7 B6 B5 B4 → 2 4 6 8 11 13 15 17 A1 A2 A3 A4 B1 B2 B3 B4 → YA1 YA2 YA3 YA4 YB1 YB2 YB3 YB4 18 16 14 12 9 7 5 3 → DATA0 DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7
GA 1 GB 19

U11 74240

7 → 13
19

U12 74244

9 → 11
19

R6 1k +5V → D.D./ACKNOWLEDGE–

P2 – 12C
P2 – 13C
P2 – 20C
P2 – 21C
P2 – 17C
P2 – 1C
P2 – 2C
P2 – 3C
P2 – 5C
P2 – 6C
P2 – 8C
P2 – 9C
P2 – 10C
P2 – 16C

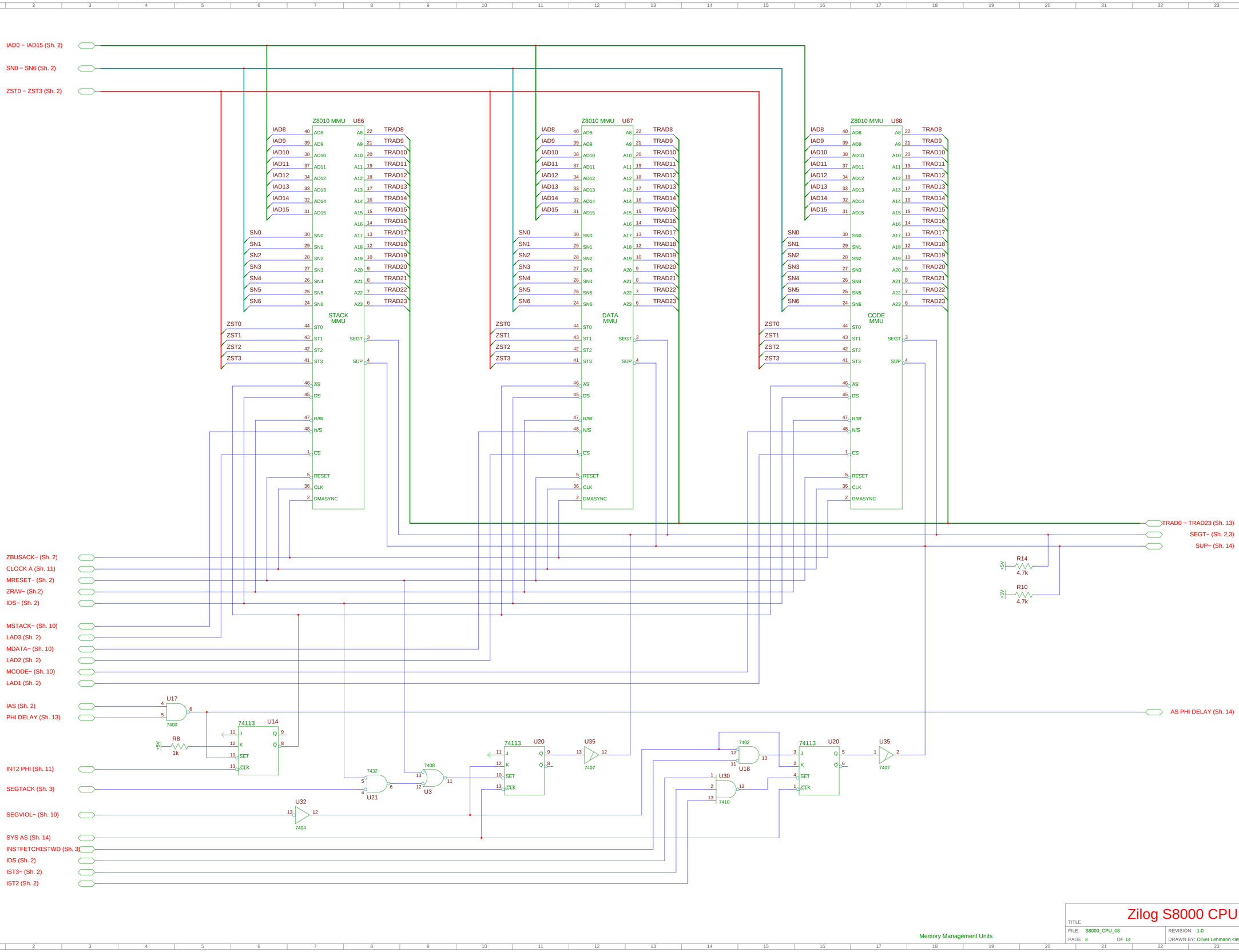
PIO 0 IEO (Sh. 14)

Serial Input/Output: Baud Rate Generators
Parallel I/O Ports

# Zilog S8000 CPU

TITLE

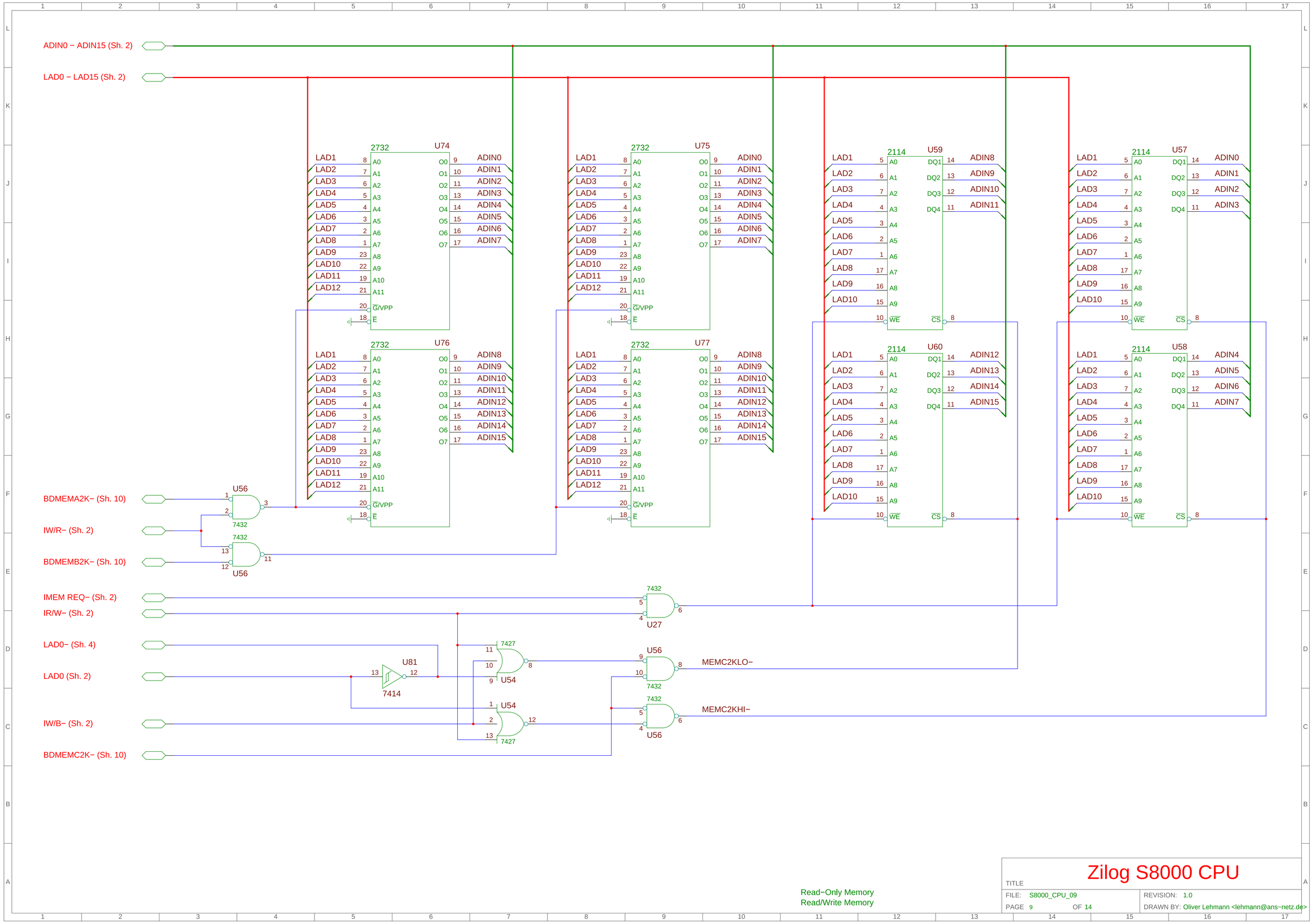
FILE: S8000_CPU_07
REVISION: 1.0
PAGE 7 OF 14
DRAWN BY: Oliver Lehmann <lehmann@ans-netz.de>

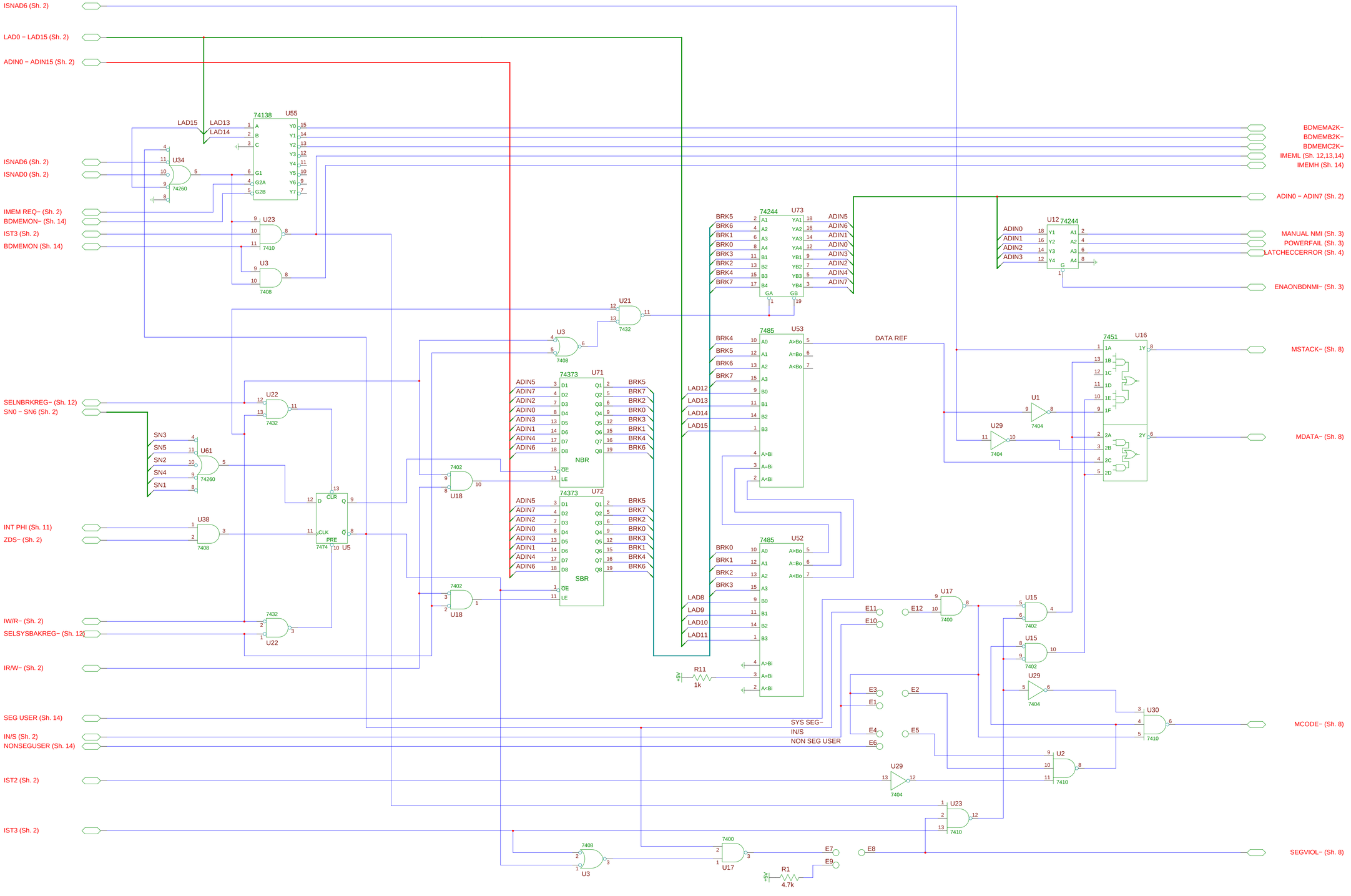



# Zilog S8000 CPU

Memory Management Units

| | |
|---|---|
| TITLE | |
| FILE: S8000_CPU_08 | REVISION: 1.0 |
| PAGE 8 OF 14 | DRAWN BY: Oliver Lehmann <lehmann@ans-netz.de> |


ADIN0 − ADIN15 (Sh. 2)
LAD0 − LAD15 (Sh. 2)
2732 U74
2732 U75
2732 U76
2732 U77
2114 U59
2114 U60
2114 U57
2114 U58
LAD1 LAD2 LAD3 LAD4 LAD5 LAD6 LAD7 LAD8 LAD9 LAD10 LAD11 LAD12
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11
G/VPP
E
O0 O1 O2 O3 O4 O5 O6 O7
ADIN0 ADIN1 ADIN2 ADIN3 ADIN4 ADIN5 ADIN6 ADIN7
ADIN8 ADIN9 ADIN10 ADIN11 ADIN12 ADIN13 ADIN14 ADIN15
DQ1 DQ2 DQ3 DQ4
WE
CS
BDMEMA2K− (Sh. 10)
IW/R− (Sh. 2)
BDMEMB2K− (Sh. 10)
U56
7432
U27
IMEM REQ− (Sh. 2)
IR/W− (Sh. 2)
LAD0− (Sh. 4)
LAD0 (Sh. 2)
IW/B− (Sh. 2)
BDMEMC2K− (Sh. 10)
U81
7414
U54
7427
MEMC2KLO−
MEMC2KHI−
Read−Only Memory
Read/Write Memory
Zilog S8000 CPU
TITLE
FILE: S8000_CPU_09
REVISION: 1.0
PAGE 9 OF 14
DRAWN BY: Oliver Lehmann <lehmann@ans−netz.de>



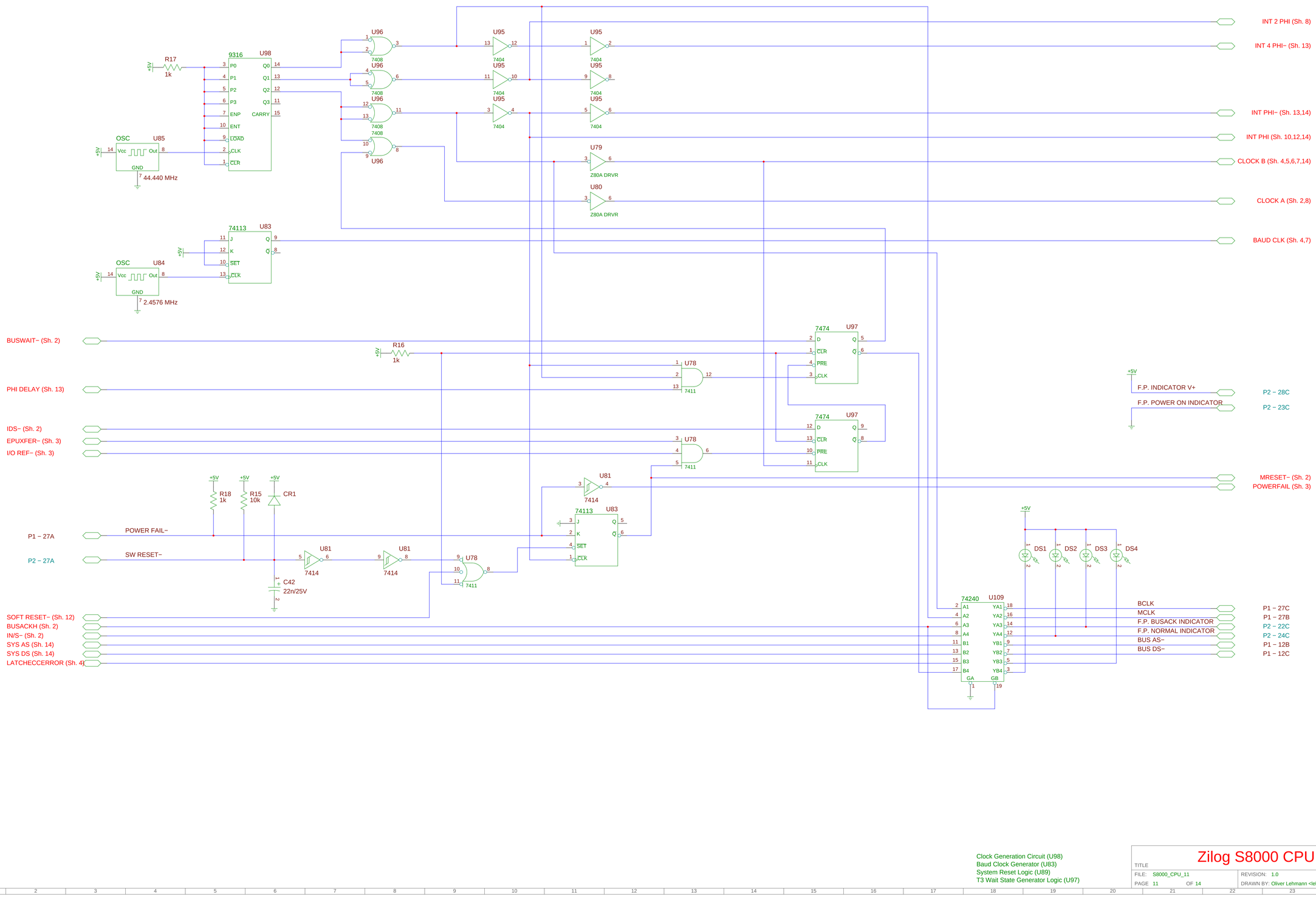

Memory Management Control Logic
Parity Error Checking: error buffer (U12)

# Zilog S8000 CPU

TITLE

FILE: S8000_CPU_10 | REVISION: 1.0

PAGE 10 OF 14 | DRAWN BY: Oliver Lehmann <lehmann@ans-netz.de>


INT 2 PHI (Sh. 8)
INT 4 PHI− (Sh. 13)
INT PHI− (Sh. 13,14)
INT PHI (Sh. 10,12,14)
CLOCK B (Sh. 4,5,6,7,14)
CLOCK A (Sh. 2,8)
BAUD CLK (Sh. 4,7)
MRESET− (Sh. 2)
POWERFAIL (Sh. 3)
P2 − 28C
P2 − 23C
P1 − 27C
P1 − 27B
P2 − 22C
P2 − 24C
P1 − 12B
P1 − 12C
BUSWAIT− (Sh. 2)
PHI DELAY (Sh. 13)
IDS− (Sh. 2)
EPUXFER− (Sh. 3)
I/O REF− (Sh. 3)
P1 − 27A
P2 − 27A
SOFT RESET− (Sh. 12)
BUSACKH (Sh. 2)
IN/S− (Sh. 2)
SYS AS (Sh. 14)
SYS DS (Sh. 14)
LATCHECCERROR (Sh. 4)
F.P. INDICATOR V+
F.P. POWER ON INDICATOR
BCLK
MCLK
F.P. BUSACK INDICATOR
F.P. NORMAL INDICATOR
BUS AS−
BUS DS−
POWER FAIL−
SW RESET−
R17 1k
R16 1k
R18 1k
R15 10k
CR1
C42 22n/25V
9316 U98
74113 U83
7474 U97
74240 U109
U78
U79
U80
U81
U85
U84
OSC
44.440 MHz
2.4576 MHz
Z80A DRVR
7404
7408
7411
7414
DS1
DS2
DS3
DS4
Clock Generation Circuit (U98)
Baud Clock Generator (U83)
System Reset Logic (U89)
T3 Wait State Generator Logic (U97)
Zilog S8000 CPU
TITLE
FILE: S8000_CPU_11
REVISION: 1.0
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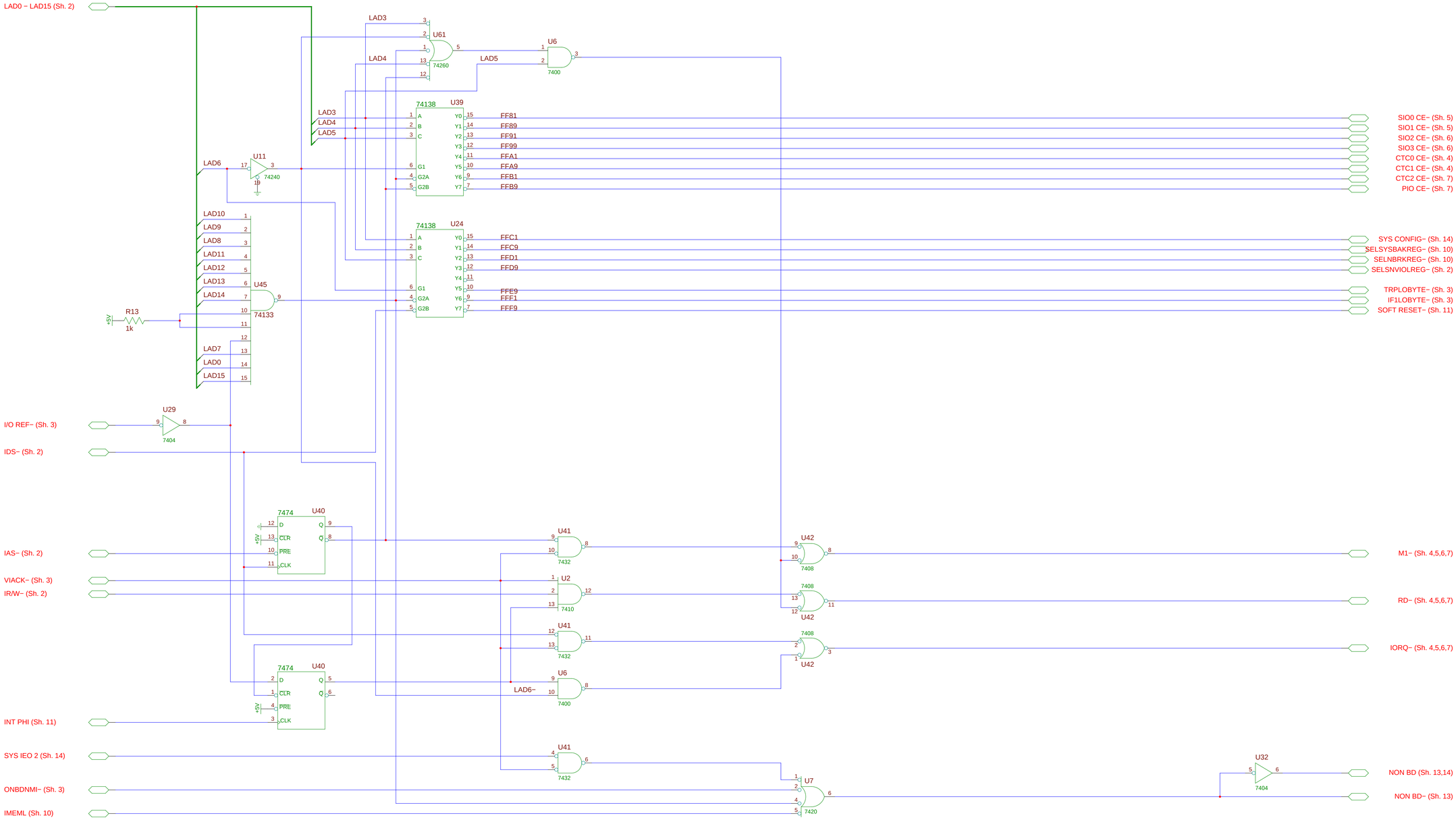
DRAWN BY: Oliver Lehmann <lehmann@ans-netz.de>




Peripheral Handshaking Logic (U24, U39)

# Zilog S8000 CPU

TITLE

FILE: S8000_CPU_12 REVISION: 1.0

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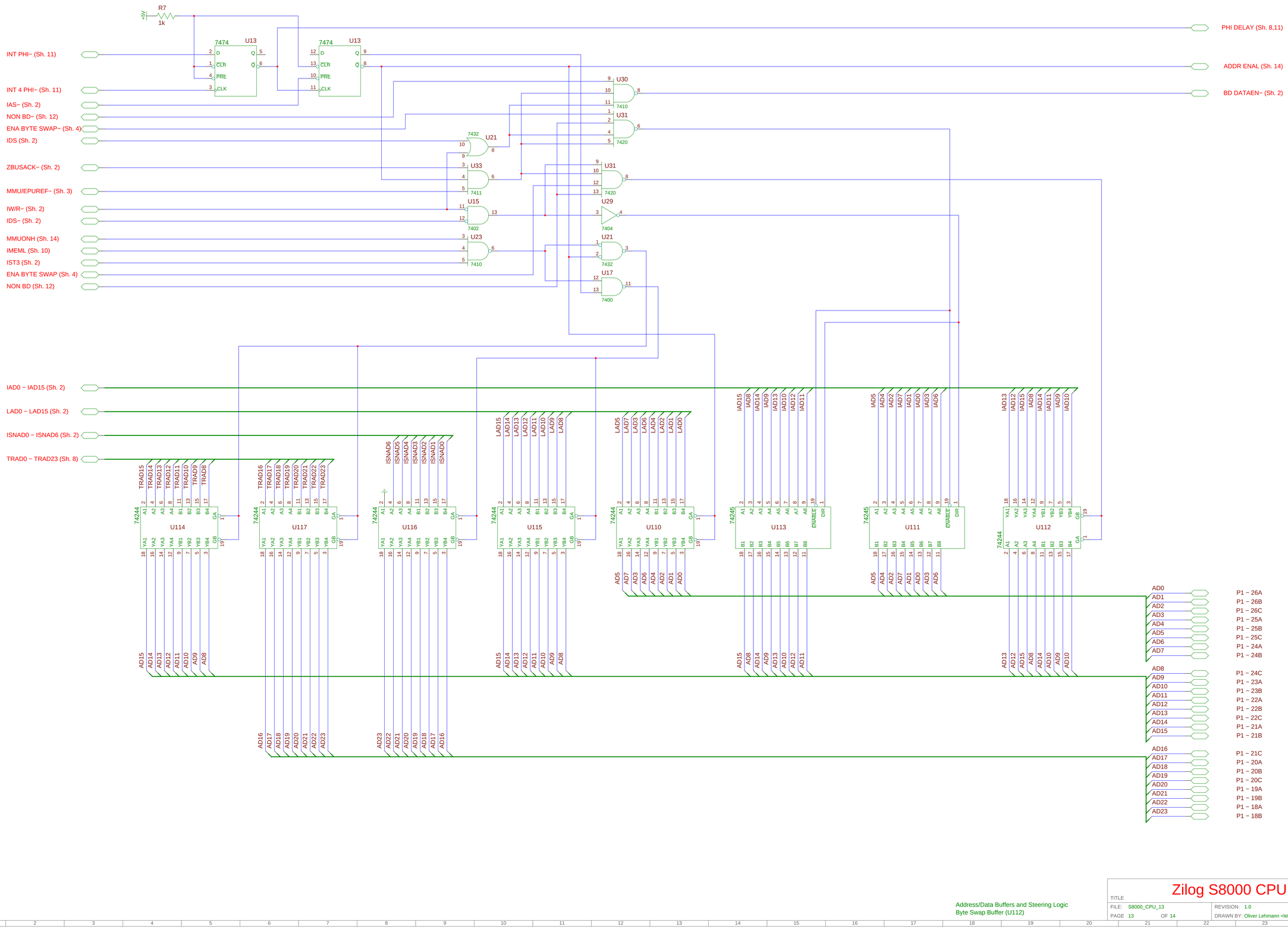
R7
+5V
1k
7474
U13
D
CLR
PRE
CLK
Q
INT PHI− (Sh. 11)
INT 4 PHI− (Sh. 11)
IAS− (Sh. 2)
NON BD− (Sh. 12)
ENA BYTE SWAP− (Sh. 4)
IDS (Sh. 2)
ZBUSACK− (Sh. 2)
MMU/EPUREF− (Sh. 3)
IW/R− (Sh. 2)
IDS− (Sh. 2)
MMUONH (Sh. 14)
IMEML (Sh. 10)
IST3 (Sh. 2)
ENA BYTE SWAP (Sh. 4)
NON BD (Sh. 12)
PHI DELAY (Sh. 8,11)
ADDR ENAL (Sh. 14)
BD DATAEN− (Sh. 2)
U30
7410
U31
7420
7432
U21
U33
7411
U15
7402
U23
U29
7404
U17
7400
IAD0 − IAD15 (Sh. 2)
LAD0 − LAD15 (Sh. 2)
ISNAD0 − ISNAD6 (Sh. 2)
TRAD0 − TRAD23 (Sh. 8)
74244
74245
U114
U117
U116
U115
U110
U113
U111
U112
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
P1 − 26A
P1 − 26B
P1 − 26C
P1 − 25A
P1 − 25B
P1 − 25C
P1 − 24A
P1 − 24B
P1 − 24C
P1 − 23A
P1 − 23B
P1 − 22A
P1 − 22B
P1 − 22C
P1 − 21A
P1 − 21B
P1 − 21C
P1 − 20A
P1 − 20B
P1 − 20C
P1 − 19A
P1 − 19B
P1 − 18A
P1 − 18B
Address/Data Buffers and Steering Logic
Byte Swap Buffer (U112)
Zilog S8000 CPU
TITLE
FILE: S8000_CPU_13
REVISION: 1.0
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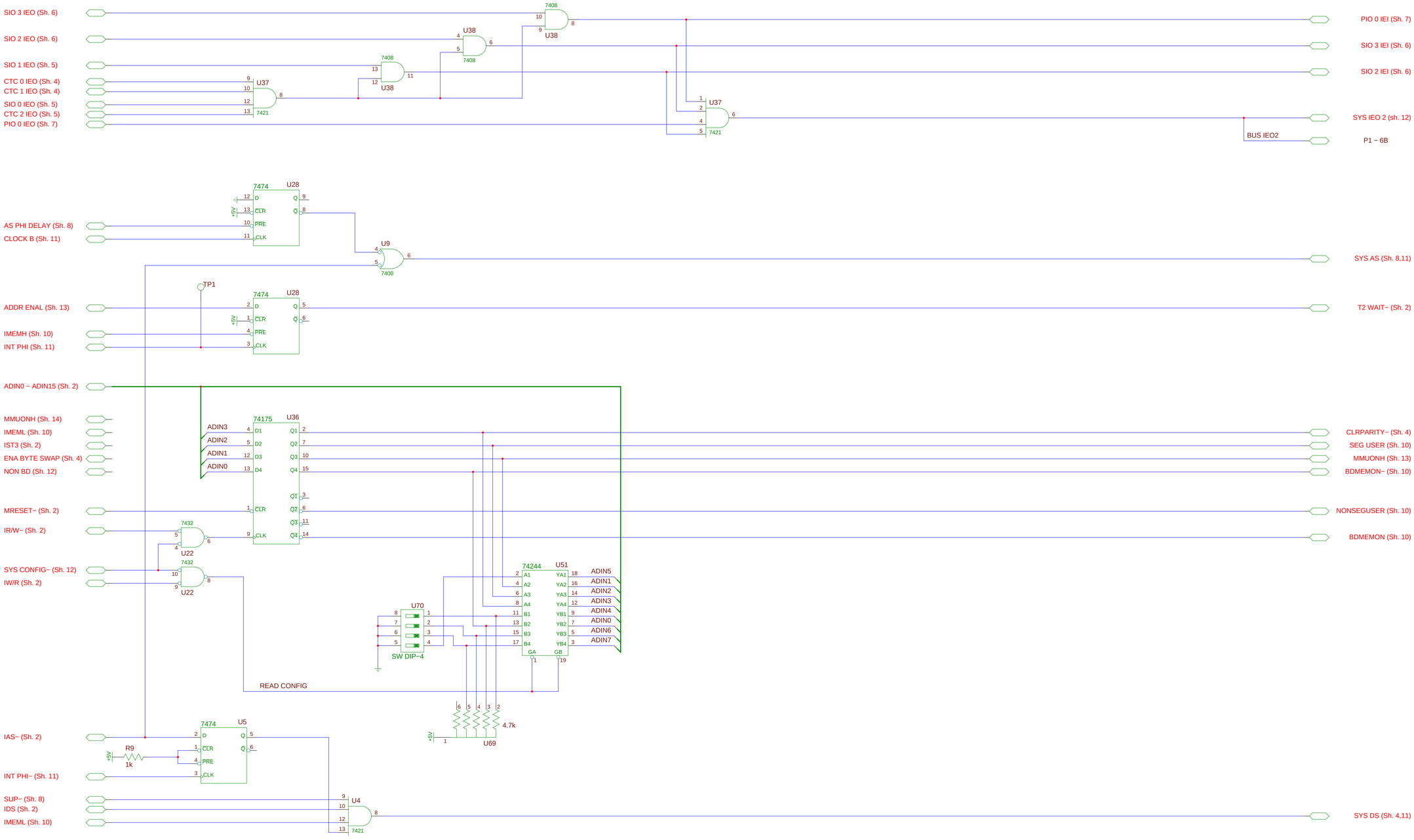
DRAWN BY: Oliver Lehmann <lehmann@ans-netz.de>


SIO 3 IEO (Sh. 6)
SIO 2 IEO (Sh. 6)
SIO 1 IEO (Sh. 5)
CTC 0 IEO (Sh. 4)
CTC 1 IEO (Sh. 4)
SIO 0 IEO (Sh. 5)
CTC 2 IEO (Sh. 5)
PIO 0 IEO (Sh. 7)
7408
U38
7421
U37
PIO 0 IEI (Sh. 7)
SIO 3 IEI (Sh. 6)
SIO 2 IEI (Sh. 6)
SYS IEO 2 (sh. 12)
BUS IEO2
P1 – 6B
AS PHI DELAY (Sh. 8)
CLOCK B (Sh. 11)
7474
U28
U9
7400
SYS AS (Sh. 8,11)
TP1
ADDR ENAL (Sh. 13)
IMEMH (Sh. 10)
INT PHI (Sh. 11)
T2 WAIT– (Sh. 2)
ADIN0 – ADIN15 (Sh. 2)
MMUONH (Sh. 14)
IMEML (Sh. 10)
IST3 (Sh. 2)
ENA BYTE SWAP (Sh. 4)
NON BD (Sh. 12)
74175
U36
ADIN3
ADIN2
ADIN1
ADIN0
CLRPARITY– (Sh. 4)
SEG USER (Sh. 10)
MMUONH (Sh. 13)
BDMEMON– (Sh. 10)
MRESET– (Sh. 2)
NONSEGUSER (Sh. 10)
IR/W– (Sh. 2)
7432
U22
BDMEMON (Sh. 10)
SYS CONFIG– (Sh. 12)
IW/R (Sh. 2)
74244
U51
ADIN5
ADIN1
ADIN2
ADIN3
ADIN4
ADIN0
ADIN6
ADIN7
U70
SW DIP–4
READ CONFIG
4.7k
U69
IAS– (Sh. 2)
R9
1k
INT PHI– (Sh. 11)
SUP– (Sh. 8)
IDS (Sh. 2)
IMEML (Sh. 10)
U4
SYS DS (Sh. 4,11)
Interrupt Priority Connection
System Configuration Register
T2 Wait State Generator Logic (U28)
Zilog S8000 CPU
TITLE
FILE: S8000_CPU_14
REVISION: 1.0
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